COMPLETE LISTING OF CLAIMS

IN ASCENDING ORDER WITH STATUS INDICATOR

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Claim 1 (currently amended) A CMOS image sensor circuit, comprising:

a first CMOS image sensor substrate, said substrate having an image sensor portion arranged in an array of pixels of rows and columns, and image sensor logic on said substrate, said image sensor logic being electrically connected to said image sensor portion, said image sensor logic including row logic associated with each of said rows individually, and chip logic associated with parts of said image sensor portion other than said rows individually, said image sensor portion having a first portion and a second portion;

said image sensor substrate formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, and second set of parallel edges including a third edge and a fourth edge;

said image sensor substrate extending between said first edge, said second edge, and said third edge, such that ~~a first area~~ said first portion of said image sensor portion is adjacent said first edge ~~of the chip includes first pixels of the image sensor, a second area adjacent said second edge of the chip includes image sensors, and a third area adjacent said third edge of the chip includes~~ and said third edge of said image sensor substrate and said second portion of said image sensor portion is adjacent said second edge and said third edge of said image sensor[[s]] substrate;

said row logic being physically located inside said image sensor in place of a plurality of pixels of the array forming said image sensor;

a pixel interpolator and said chip driver circuitry located between said ~~image area and~~ first portion and said second portions of said image sensor portion and said fourth edge of said image sensor substrate; and

a second CMOS image sensor substrate configured similarly to said first CMOS image sensor substrate and abutted to one of said edges of said first CMOS image sensor substrate.

Claim 2. (original) A circuit as in claim 1 wherein said row logic is formed in place of two columns of the array forming the active pixel sensor.

Claim 3. (original) A circuit as in claim 1 wherein said image sensor extends within two pixel pitches of first, second, and third edges of the chip.

Claim 4. (original) A circuit as in claim 3 wherein said first and second edges are perpendicular to said third and fourth edges.

Claim 5. (original) A circuit as in claim 1 further comprising an interpolating element, operating to interpolate pixels which would have impinged on areas of said image sensor portions.

Claim 6. (original) A circuit as in claim 1 wherein said row logic is in the center of the plurality of pixels forming the image sensor.

Claim 7. (original) A circuit as in claim 1 wherein the ends of the image sensor includes a guard ring.

Claim 8. (original) A method of operating a large format image sensor, comprising:

first obtaining an image sensor chip which has first and second edges where said image sensor comes within two pixel pitches of said first and second edges, and includes

row selecting logic in place of a plurality of central pixels of the image sensor;

abutting said image sensor chip against a similar image sensor chip of corresponding construction; and

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interpolating missing pixels caused by both said row select logic and by spaces between said image sensor chips.

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Claim 9. (previously presented) A CMOS imager, comprising:

a first CMOS image sensor having an image sensor portion arranged in an array of rows and columns, said first CMOS image sensor formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, and second set of parallel edges including a third edge and a fourth edge;

said first CMOS image sensor having a control portion and a centralized row-local control portion, said centralized row-local control portion being physically located inside said image sensor in place of a plurality of pixels of the array forming said image sensor thereby forming at least two image sensor areas; and

said control portion including a pixel interpolator located between said at least two image sensor area and one of said edges of said image sensor.

Claim 10. (previously presented) The CMOS imager according to claim 9, further comprising a second CMOS image sensor configured similarly to said first CMOS image sensor and abutted to one of said edges of said first CMOS image sensor.

Claim 11. (previously presented) A method of fabricating a CMOS imager comprising:

fabricating at least two CMOS image sensors having an image sensor portion arranged in an array of rows and columns, said at least two CMOS image sensors formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, and second set of parallel edges including a third edge and a fourth edge, said at least two image sensor having a control portion and a centralized row-local control portion, said centralized row-local control portion being physically located inside said image sensor in place of a plurality of pixels of the array forming said image sensor thereby forming at least two image sensor areas, said control portion including a pixel interpolator located between said at least two image sensor area and one of said edges of said image sensor;

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abutting said at least two CMOS image sensors together; and

integrating said control portions of said at least two CMOS image sensors such that said at least two CMOS image sensors function as a single CMOS imager.

Claim 12. (previously presented) The method of fabricating according to claim 11, further comprising interpolating, using said pixel interpolator of said control portion, missing pixels caused by said centralized row-local control portion and by spaces between said at least two image sensors.

Claim 13. (new) A CMOS image sensor circuit, comprising:

a first CMOS image sensor substrate, said substrate having an image sensor portion arranged in an array of pixels of rows and columns, and image sensor logic on said substrate, said image sensor logic being electrically connected to said image sensor portion, said image sensor logic including row logic associated with each of said rows individually, and chip logic associated with parts of said image sensor portion other than said rows individually, said image sensor portion having a first portion and a second portion;

said image sensor substrate formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, and second set of parallel edges including a third edge and a fourth edge;

said image sensor substrate extending between said first edge, said second edge, and said third edge, such that said first portion of said image sensor portion is adjacent said first edge and said third edge of said image sensor substrate and said second portion of said image sensor portion is adjacent said second edge and said third edge of said image sensor substrate;

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said row logic being physically located inside said image sensor in place of a plurality of pixels of the array forming said image sensor; and

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a second CMOS image sensor substrate configured similarly to said first CMOS image sensor substrate and abutted to one of said edges of said first CMOS image sensor substrate.

Claim 14. (new) The CMOS image sensor circuit according to claim 13, further comprising a pixel interpolator and said chip driver circuitry located between said first portion and said second portions of said image sensor portion and said fourth edge of said image sensor substrate.

Claim 15. (new) A method of operating a large format image sensor, comprising:

first obtaining an image sensor chip which has first and second edges where said image sensor comes within two pixel pitches of said first and second edges, and includes row selecting logic in place of a plurality of central pixels of the image sensor; and

abutting said image sensor chip against a similar image sensor chip of corresponding construction.

Claim 16. (new) The method according to claim 15, further comprising interpolating missing pixels caused by both said row select logic and by spaces between said image sensor chips.

Claim 17. (new) A method of fabricating a CMOS imager comprising fabricating at least two CMOS image sensors having an image sensor portion arranged in an array of rows and columns, said at least two CMOS image sensors formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, and second set of parallel edges including a third edge and a fourth edge, said at least two image sensor having a control portion and a centralized row-local control portion, said centralized row-local control portion being physically located inside said image sensor in place of a plurality of pixels of the array forming said image sensor thereby forming at least two image sensor areas, said control portion including a pixel interpolator located between said at least two image sensor area and one of said edges of said image sensor.

Claim 18. (new) The method according to claim 17, further comprising:

abutting said at least two CMOS image sensors together; and

integrating said control portions of said at least two CMOS image sensors such that said at least two CMOS image sensors function as a single CMOS imager.